PerfectVIPs
Right Tools... Perfect Chip

NVM EXPRESS 1.0 VIP

DATASHEET
Rev. 1

GENIE-NVMe1^{TM}

NVM EXPRESS 1.0 VERIFICATION IP

OVERVIEW

The Genie-NVMe^{TM} Verification IP Products provide the most robust verification solution for NVMe 1.0 based designs. The intelligent **Verification Engine**, developed with latest technology UVM to reduce design risk, verification time and project costs. Genie-NVMe^{TM} Verification IP can be plugged with PCIe and also plugged with other Interface or Bus.

The **Genie-NVMe^{TM} VIP** provides a quick and efficient way to verify any NVMe based design. It supports the NVMe 1.0 specification. Genie-NVMe provides a complete verification solution that includes multi-language support and UVM methodology.

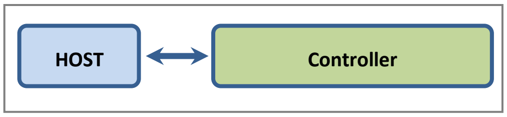

Fig. 1: Simple Host/Controller Design

The Genie-NVMe VIP provides:

- Bus Functional Models
- Directed and Random Transaction Generator
- Packet & Order set Generator
- Error Injector
- Reusable verification components
- Monitor/Checker
- Verbosity based report generation

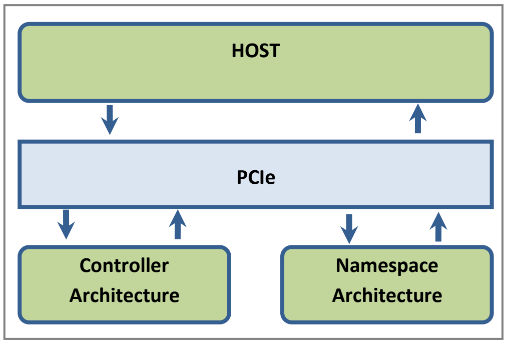

Fig. 2: Host and controller Configuration

FEATURES

- Compliant with NVMe Standard 1.0b
- Support for up to 64K I/O queues, with each I/O queue supporting up to 64K commands.
- Priority associated with each I/O queue with well-defined arbitration mechanism
- Reset , Initialization and Shutdown Process
- Admin Command Set Supported
- I/O (NVM) command Set
- Queue Management supported
- Command Arbitration
- Supports UVM methodology
- Host and Controller can be connected through other interfaces
- Host and Controller can be used with PCIe (as shown in fig.2)
- Comprehensive Compliance Suite

PRODUCT DETAILS

Host Operation: Host software presents command to the controller through pre-allocation Submission Queues. The admin queue is configured by setting the Admin Queue Attributes, Admin Submission Queue Base Address, and Admin Completion Queue Base Address to appropriate value. The arbitration mechanism, memory page size and I/O command set is selected first. Host randomizes the command, fill the I/O queues and alert the controller to new commands to execute through SQ Tail Doorbell register writes. After processing command controller sends back Completion command to Host. Host writes Doorbell to release completion entry.

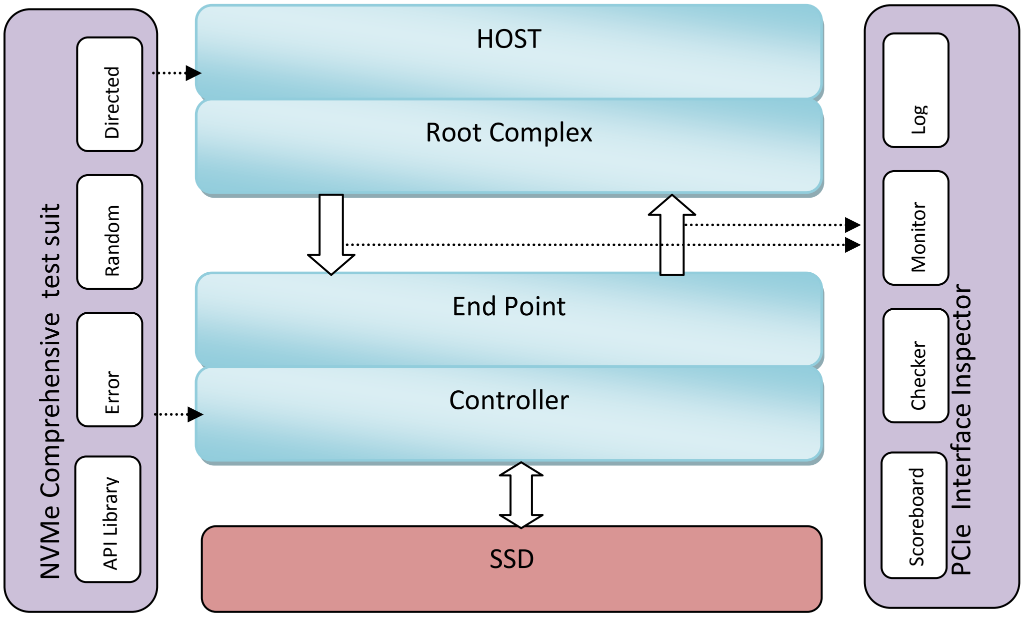

Fig 3 : NVMe Env with PCIe

ControllerOperation: Controller initially set its all Controller registers as per users configuration. Host configures the controller and once controller is out of its initialization process, It waits for host to write in tail doorbell registers. Based on doorbell register write controller fetch commands from host. Based on selected arbitration controller process the commands. After executing command, controller writes a completion queue entry, the controller indicates the most recent SQ entry that has been fetched.

BENEFITS

- Guarantees compliance to NVMe 1.0b specification
- Reduces test development effort
- System level verification
- Shortens verification schedule
- Reduces overall design and verification costs
- Plug-and-play into all major simulation environments

SUPPORTED SIMULATORS: ALDEC CADENCE MENTOR SYNOPSYS